What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a molding layer over a semiconductor wafer;

patterning the molding layer to form a plurality of storage node holes, wherein the plurality of storage node holes include at least one first storage node hole formed on an effective chip area and at least one second storage node hole formed on an edge chip area;

forming first and second storage nodes in the first and second storage node holes, respectively;

forming a photoresist pattern that covers the edge chip area; and

selectively etching the molding layer, using the photoresist pattern as an etching mask, to expose portions of the first storage nodes.

2. The method of claim 1, wherein the photoresist pattern exposes the effective chip area.

3. The method of claim 1, wherein selectively etching the molding layer is performed after forming the photoresist pattern that covers the edge chip area.

4. The method of claim 1, further comprising:

sequentially forming a lower interlayer dielectric layer and an etch stop layer on the semiconductor wafer prior to formation of the molding layer; and

forming a plurality of contact plugs electrically connected to the semiconductor wafer, wherein the contact plugs include at least one first buried contact plug formed in the effective chip area, and at least one second buried contact plug formed in the edge chip area.

5. The method of claim 4, wherein the etch stop layer is formed of a material layer having an etch selectivity with respect to the lower interlayer dielectric layer and the molding layer.

6. The method of claim 5, wherein the etch stop layer comprises a silicon nitride layer.

7. The method of claim 1, wherein the first and second storage nodes have a cylindrical shape, the method further comprising:

filling the first and second cylindrical storage nodes with sacrificial layer patterns; and

removing the sacrificial layer patterns in the first cylindrical storage nodes when the molding layer is etched.

8. The method of claim 1, further comprising:

removing the photoresist pattern;

sequentially forming a dielectric layer and a plate conductive layer overlying the first and second storage nodes; and

patterning the plate conductive layer and the dielectric layer to form plate electrodes and dielectric layer patterns.

9. The method of claim 8, further comprising:

forming a first upper interlayer dielectric layer overlying the plate electrodes;

partially etching the first upper interlayer dielectric layer on the plate electrodes to form a first planarized upper interlayer dielectric layer;

forming a second upper interlayer dielectric layer on the first planarized upper interlayer dielectric layer; and

planarizing the first and second upper interlayer dielectric layers to form a second planarized upper interlayer dielectric layer.

10. The method of claim 9, wherein the first upper interlayer dielectric layer comprises a flowable dielectric layer.

11. The method of claim 10, wherein the flowable dielectric layer comprises a borophosphosilicate glass (BPSG) layer.

12. The method of claim 9, wherein the second upper interlayer dielectric layer is formed of a chemical vapor deposition (CVD) oxide layer.

13. The method of claim 9, wherein planarizing the first and second upper interlayer dielectric layers comprises etching back.

14. A semiconductor device produced by a process comprising:

forming a molding layer over a semiconductor wafer;

patterning the molding layer to form a plurality of storage node holes, wherein the plurality of storage node holes include at least one first storage node hole formed on an effective chip area and at least one second storage node hole formed on an edge chip area;

forming first and second storage nodes in the first and second storage node holes, respectively;

forming a photoresist pattern that covers the edge chip area; and

selectively etching the molding layer, using the photoresist pattern as an etching mask, to expose portions of the first storage nodes.

15. The semiconductor device of claim 14 produced by a process further comprising:

sequentially forming a lower interlayer dielectric layer and an etch stop layer on the semiconductor wafer prior to formation of the molding layer; and

forming a plurality of contact plugs electrically connected to the semiconductor wafer, wherein the contact plugs include at least one first buried contact plug formed in the effective chip area, and at least one second buried contact plug formed in the edge chip area.

16. The semiconductor device of claim 15, wherein the etch stop layer is a material layer having an etch selectivity with respect to the lower interlayer dielectric layer and the molding layer.

17. The semiconductor device of claim 16, wherein the etch stop layer is a silicon nitride layer.

18. The semiconductor device of claim 14 produced by a process further comprising, wherein the first and second storage nodes have a cylindrical shape:

filling the first and second cylindrical storage nodes with sacrificial layer patterns; and

removing the sacrificial layer patterns in the first cylindrical storage nodes when the molding layer is etched.

19. The semiconductor device of claim 14 produced by a process further comprising:

removing the photoresist pattern;

sequentially forming a dielectric layer and a plate conductive layer overlying the first and second storage nodes; and

patterning the plate conductive layer and the dielectric layer to form plate electrodes and dielectric layer patterns.

20. The semiconductor device of claim 19 produced by a process further comprising:

forming a first upper interlayer dielectric layer on the wafer having the plate electrodes;

partially and selectively etching the first upper interlayer dielectric layer on the plate electrodes to form a first planarized upper interlayer dielectric layer;

forming a second upper interlayer dielectric layer on the first planarized upper interlayer dielectric layer; and

planarizing the first and second upper interlayer dielectric layers to form a second planarized upper interlayer dielectric layer.

21. The semiconductor device of claim 20, wherein the first upper interlayer dielectric layer is a flowable dielectric layer.

22. The semiconductor device of claim 22, wherein the flowable dielectric layer is a borophosphosilicate glass (BPSG) layer.

23. The semiconductor device of claim 20, wherein the second upper interlayer dielectric layer is a chemical vapor deposition (CVD) oxide layer.

24. The semiconductor device of claim 14, wherein the photoresist pattern exposes the effective chip area.

25. The semiconductor device of claim 14, wherein selectively etching the molding layer is performed after forming the photoresist pattern that covers the edge chip area.